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(Not for submission under 37 CFR 1.99)

Application Number		10786874
Filing Date		2004-02-24
First Named Inventor	Haw-minn Lu	
Art Unit	2616	
Examiner Name	Wellington Chin	
Attorney Docket Number		

/Y.Z./	1	PATEL, et al., "Performance of processor-memory interconnections for multiprocessors", IEEE Transactions on Computers, Oct. 1981, pp. 771-780, vol. 30, no. 10, IEEE, US	<input type="checkbox"/>
/Y.Z./	2	GOKE, et al., "Banyan Network for partitioning multiprocessor systems," First Annual International Symposium on Computer Architecture, December 1973, pp. 21-28, ACM Press, US	<input type="checkbox"/>
/Y.Z./	3	KUMAR, et al., "Augmented shuffle-exchange multistage interconnection networks". Computer, June 1987, pp.30-40, vol. 20, no. 6, IEEE, US	<input type="checkbox"/>
/Y.Z./	4	ADAMS, et al., "The Extra Stage Cube: A Fault-Tolerant Interconnection Network for Supersystems," IEEE Transactions on Computers, May 1982, pp. 443-454, vol. 31, no. 5, IEEE, US	<input type="checkbox"/>
/Y.Z./	5	BENES, "Permutation Groups, Complexes, and Rearrangeable Connecting Networks, Bell System Telephone Journal, July 1964, pp. 1619-1640, vol. 44, AT&T, US	<input type="checkbox"/>
/Y.Z./	6	HAMID, et al., "A new fast control mechanism for Benes rearrangeable interconnection network useful for supersystems," Transactions of the Institute of Electronics, Information and Communication Engineers, October 1987, p.997-1008, vol. E70, no. 10, IEICE, Japan.	<input type="checkbox"/>
/Y.Z./	7	DUDGEON, et al., "Multidimensional Signal Processing," 1984, pp. 60-111, Prentice Hall, Englewood Cliffs, New Jersey."	<input type="checkbox"/>
/Y.Z./	8	OPPENHIEM, et al., "Digital Signal Processing," 1975, pp. 284-328, Prentice Hall, Englewood Cliffs, New Jersey.	<input type="checkbox"/>

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/Y.Z./	1	CIZEK, et al. "Tradeoff Between Cost and Reliability in Packet Switching MultiStage Interconnection Networks," AFRICON '92 Proceedings., 3rd AFRICON Conference, 22-24 Sept. 1992, pp. 365 -368, IEEE, South Africa (Reprinted US).	<input type="checkbox"/>
/Y.Z./	2	AGRAWAL, "Testing and Fault-Tolerance of Multistage Interconnection Networks," Computer, Apr. 1982, pp. 41-53, vol. 15, no. 4, IEEE, US	<input type="checkbox"/>
/Y.Z./	3	BHUYAN, et al., "Design and Performance of Generalized Interconnection Networks." IEEE Transactions on Computers, Dec. 1983, pp. 1081-1090, vol. 32, no. 12, IEEE, US	<input type="checkbox"/>
/Y.Z./	4	BLAKE, et al., "Multistage Interconnection Network Reliability," IEEE Transactions on Computers, Nov. 1989, pp. 1600-1603, vol. 38, no. 11, IEEE, US	<input type="checkbox"/>
/Y.Z./	5	CHIN, et al., "Packet Switching Networks for Multiprocessors and Data Flow Computers," IEEE Transactions on Computers, Nov. 1984, pp. 991-1003, vol. 33, no. 11, IEEE, US	<input type="checkbox"/>
/Y.Z./	6	KUMAR, et al., "Failure Dependent Performance Analysis of a Fault-Tolerant Multistage Interconnection Network," IEEE Transactions on Computers, Dec. 1989, pp. 1703-1713, vol. 38, no. 12, IEEE, US	<input type="checkbox"/>
/Y.Z./	7	TZENG, et al., "Realizing Fault-Tolerant Interconnection Network via Chaining," IEEE Transactions on Computers, Apr. 1988, pp. 458-462, vol. 37, no. 4, IEEE, US	<input type="checkbox"/>
/Y.Z./	8	VARMA, et al., "Fault-Tolerant Routing in Multistage Interconnection Networks," IEEE Transactions on Computers, Mar. 1989, pp. 385-393, vol. 38, no. 3, IEEE, US	<input type="checkbox"/>

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